AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, including a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit;

the control circuit includes: a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and

the control circuit outputs the output signals of the two NOR circuits as control signals.

2. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, including a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit;

the control circuit includes: a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively; and

the control circuit outputs the output signals of the respective NOR circuits and the inverters as control signals.

3. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit, wherein:

the control circuit includes: a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a NOR circuit fed from the second power supply, which receives a non-

inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and

the control circuit outputs the output signals of the two NOR circuits as control signals.

4. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit, wherein:

the control circuit includes: a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively; and

the control circuit outputs the output signals of the respective NOR circuits and the inverters as control signals.

5. (previously presented): The level shift circuit claimed in one of claims 1 to 4, wherein the NOR circuit has CMOS circuitry, and each PMOS connected to the level shift input signal is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

6. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, including a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit;

the control circuit includes: a NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and

the control circuit outputs the output signals of the two NAND circuits as control signals.

7. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit, wherein:

the control circuit includes: a NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and

the control circuit outputs the output signals of the two NAND circuits as control signals.

8. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit, wherein:

the control circuit includes: a NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level

shift output signals; a NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NAND circuits, respectively; and

the control circuit outputs the output signals of the respective NAND circuits and the inverters as control signals.

9. (previously presented): The level shift circuit claimed in one of claims 6 to 8, wherein the NAND- circuit has CMOS circuitry, and each PMOS connected to the level shift input signal is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

10. (currently amended): The level shift circuit claimed in one of claims ~~1 to 4 and 6 to 8~~ 1,2,3,4,6,7, or 8, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs and a differential NMOS switch including a plurality of NMOSs:

wherein the source of each PMOS is connected to the second power supply, the gate of each PMOS is connected to the level shift output through the drain of another PMOS, the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input.

11. (currently amended): The level shift circuit claimed in one of claims ~~1 to 4 and 6 to 8~~ 1,2,3,4,6,7, or 8, wherein the pull-up and/ or pull-down circuit comprises: a plurality of PMOSs

each having a source connected to the second power supply, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output; and a plurality of NMOSs each having a source connected to the ground voltage GND, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output.

12. (currently amended): The level shift circuit claimed in one of claims ~~1 to 4 and 6 to 8~~ 1,2,3,4,6,7, or 8, wherein the level shift core circuit comprises:

a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output;

a plurality of PMOS switches each having a source connected to the drain of one of the PMOSs, a gate connected to the level shift input and a drain connected to the level shift output; and

a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to the level shift output and a gate connected to the level shift input.

13. (currently amended): The level shift circuit claimed in one of claims ~~1 to 4 and 6 to 8~~ 1,2,3,4,6,7, or 8, wherein the level shift core circuit comprises:

a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output through the drain of another PMOS;

a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to the level shift output and a gate connected to the level shift input; and

NMOSs each having a drain connected to the first power supply, a gate connected to the level shift input and a source connected to the level shift output.